Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): An output circuit, comprising:

a first switch for supplying a first external power to be used as a second external power or shutting off the supply of the first external power, according to a control signal;

an output buffer for outputting a signal ~~keeping the~~ having a potential of the second external power or a ground potential, depending on an input signal, an enable signal and the control signal;

an output driver for outputting a signal ~~keeping~~ having the potential of the second external power or the ground potential depending on the output signal of the output ~~butter~~ buffer;

a second switch for allowing one of input terminals of the output driver to have the potential of the first external power according to the control signal; and

a third switch for allowing the other of the input terminals of the output driver to have the ground potential according to the control signal.

Claim 2 (Original): The output circuit as claimed in claim 1, wherein the control signal is a signal that is applied as different potential states in a normal operating mode and a deep power down mode.

Claim 3 (Original): The output circuit as claimed in claim 1, wherein the first switch is a PMOS transistor that is driven according to the control signal.

Claim 4 (Currently Amended): The output circuit as claimed in claim 1, wherein the output buffer comprises:

a first input means for receiving the input signal and the enable signal ~~as an input~~;

a second input means for receiving the input signal and the enable signal ~~as an input~~;

a first driving means for outputting the potential of the second external power or ~~the signal of~~ the ground potential to a first node, according to the control signal and ~~the~~ an output signal of the first input means; and

a second driving means for outputting the potential of the second external power or ~~the signal of~~ the ground potential to a second node, according to the control signal and [[the]] an output signal of the second input means.

Claim 5 (Currently Amended): The output circuit as claimed in claim 4, wherein the first input means comprises:

a first inverter for inverting the input signal;

a second inverter for inverting the enable signal; and

a NOR gate for performing a NOR operation [[for]]of the output signal of the first inverter and the output signal of the second inverter.

Claim 6 (Currently Amended): The output circuit as claimed in claim 4, wherein the second input means comprises:

an inverter for inverting the input signal; and

a NAND gate for performing a NAND operation [[for]]of the output signal of the inverter and the enable signal.

Claim 7 (Currently Amended): The output circuit as claimed in claim 4, wherein the first driving means comprises:

a level shifter for outputting an output signal having the potential of the second external power or ~~the signal of~~ the ground potential according to the output signal of the first input means;

[[a]]an NMOS transistor connected between the output terminal of the first level shifter and the ground terminal and driven by the control signal;

a PMOS transistor for supplying the second external power according to the control signal; and

an inverter for outputting the potential of the second external power supplied through the PMOS transistor or ~~the signal of~~ the ground potential, according to the output signal of the [[first]]level shifter.

Claim 8 (Currently Amended): The output circuit as claimed in claim 4, wherein the second driving means comprises:

a level shifter for outputting the potential of the second external power or ~~the signal of~~ the ground potential according to the output signal of the second input means; and

an inverter for inverting the output signal of the level shifter to output the potential of the second external power or ~~the signal of~~ the ground potential.

Claim 9 (Currently Amended): The output circuit as claimed in claim 4, further comprising [[a]]an NMOS transistor for keeping the potential of [[the]]an input terminal of the first driving means to be the ground potential, according to the control signal.

Claim 10 (Currently Amended): The output circuit as claimed in claim 4, further comprising [[a]]an NMOS transistor for keeping the potential of the input terminal of the second driving means to be the ground potential, according to the control signal.

Claim 11 (Currently Amended): The output circuit as claimed in claim 1, wherein the second switch comprises:

an inverter for outputting an output signal having the potential of the first external power or ~~the signal of~~ the ground potential according to the control signal; and

a PMOS transistor for supplying the first external power to a first node depending on the output signal of the inverter.

Claim 12 (Currently Amended): The output circuit as claimed in claim 1, wherein the third switch is [[a]]an NMOS transistor connected between a second node and the ground terminal and driven by the control signal.

Claim 13 (Currently Amended): An output circuit, comprising:

a first switch for supplying a first external power to be used as a second external power in a normal operating mode and shutting off the supply of the first external power in a deep power down mode, according to a control signal;

an output buffer for outputting a signal ~~keeping the~~ having a potential of the second external power or [[the]]a ground potential according to an enable signal and the control signal in the normal operating mode, wherein the output buffer is floated in the deep power down mode;

an output driver for outputting a signal ~~keeping~~ having the potential of the second external power or the ground potential according to the output signal of the output buffer in the normal operating mode;

a second switch for allowing one of input terminals of the output driver to have the potential of the first external power in the deep power down mode; and

a third switch for allowing the other of the input terminals of the output driver to have the ground potential in the deep power down mode.

Claim 14 (Currently Amended): An output circuit, comprising:

a first switch for supplying a first external power to be used as a second external power in a normal operating mode and shutting off the supply of the first external power in a deep power down mode, according to a control signal;

a first input means for receiving a global input/output signal and an output enable signal ~~as an input~~;

a second input means for receiving the global input/output signal and the output enable signal ~~as an input~~;

a first driving means for outputting [[the]]a potential of the second external power supplied through the first switch or ~~a signal of~~ the ground potential to a first node according to [[the]]an output signal of the first input means in the normal operating mode, wherein the first driving means is floated in the deep power down mode;

a second driving means for outputting the potential of the second external power supplied through the first switch or ~~the signal of~~ the ground potential to a second node according to [[the]]an output signal of the second input means in the normal operating mode, wherein the second driving means is floated in the deep power down mode;

a second switch for supplying the first external power to the first node according to the control signal in the deep power down mode;

a third switch for controlling the potential of the second node to become the ground potential according to the control signal in the deep power down mode; and

an output driver for outputting the potential of the second external power supplied through the first switch or ~~the signal of~~ the ground potential to an output terminal depending on the potential of the first node and the potential of the second node in the normal operating mode.